Set Items Description
S1 25031 S (PROTECT? OR ENCRYPT? OR CRYPTO? OR CRYPTANALY? OR CIPHER? OR CYPHER? OR ENCIPHER? OR SCRAMBL? OR DECRYPT? OR DECIPHER? OR UNENCRYPT? OR UNSCRAMBL? OR KEY? ?)(3N)(TIME? ? OR TIMING OR TIMESTAMP? ? OR CLOCK??? OR INTERVAL? ?)
S2 1471 S S1(5N)(GROUP? ? OR COLLECTION? ? OR MULTIPLE? ? OR MANIFOLD OR NUMEROUS OR MULTIPL? OR MULTITUDE OR SEVERAL OR MANY OR PLURAL? OR VARIET? OR RANGE? ? OR ASSORT???? OR DIVERSE)
S3 31 S S2(5N)(LEVEL? ? OR BRANCH? ? OR SEGMENT? ?)
S4 196474 S (LOWER OR UPPER OR SECOND)(2N)(LIMIT? ? OR LIMITATION? ? OR LEVEL? ? OR BOUND? OR CONSTRAIN? OR CAP OR CAPS OR CUTOFF? ? OR CUT()OFF? ? OR THRESHOLD? ?)
S5 5 S S3 AND S4

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Subject summary

? t /3,k/all
5/3,K/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0013278876 & & *Drawing available*
WPI Acc no: 2003-365154/200335
XRPX Acc No: N2003-291539
Apparatus for protecting electrical load from parallel arc fault has semiconductor switch operated in three modes according to current level
Patent Assignee: EATON CORP (EAYT)
Inventor: BERKOPEC W E; HASTINGS J K; JAHN R R; KRISTIC S; KRSTIC S; PAHL B; ZUERCHER J C
Patent Family (10 patents, 37 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 1298770	A2	20030402	EP 200221848	A	20020929	200335	B
CA 2405135	A1	20030328	CA 2405135	A	20020925	200335	E
US 20030063420	A1	20030403	US 2001967116	A	20010928	200335	E
JP 2003189459	A	20030704	JP 2002284796	A	20020930	200353	E
US 6590757	B2	20030708	US 2001967116	A	20010928	200353	E
CN 1417913	A	20030514	CN 2002149899	A	20020928	200355	E
BR 200204291	A	20030916	BR 20024291	A	20020927	200369	E
MX 2002009607	A1	20030301	MX 20029607	A	20020927	200413	E
TW 575987	A	20040211	TW 2002121314	A	20020918	200454	E
MX 226360	B	20050217	MX 20029607	A	20020927	200565	E

Priority Applications (no., kind, date): US 2001967116 A 20010928

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 1298770	A2	EN	10	4		
Regional Designated States,Original	AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR					
CA 2405135	A1	EN				
JP 2003189459	A	JA	9			
BR 200204291	A	PT				
TW 575987	A	ZH				

Alerting Abstract ...after a set time, and a third mode when the current is greater than the second threshold and the switch is alternately pulsed between states to limit the current through the load to less than the second threshold. The control circuit measures the pulses to determine whether a parallel arc fault has occurred... Original Publication Data by AuthorityArgentinaPublication No. ...Original Abstracts:until the circuit is specifically reset. When the current to the equipment exceeds a greater second threshold, a pulsed signal alternately places the semiconductor switch (18) in conductive and non-conductive states so that the average... ... until the circuit is specifically reset. When the current to the equipment exceeds a greater second threshold, a pulsed signal alternately places the semiconductor switch (18) in conductive and non-conductive states so that the average current applied to the equipment (14) is within an acceptable level. The pulses are measured... ... 14). When the current to the equipment exceeds a first threshold for a predefined period of time, the semiconductor switch (18) is rendered non-conductive until the circuit is specifically reset. When the current to the equipment exceeds a greater second threshold, a pulsed signal alternately places the semiconductor switch (18) in conductive and non-conductive states... ... an acceptable level. The pulses are measured to determine whether a parallel arc fault has occurred. When the measured pulses (74) are within a predetermined range, a parallel arc fault is declared... ...Claims:when the magnitude of current is greater than the first threshold and less than a second threshold wherein the semiconductor switch (18) is rendered non-conductive after a predefined period of time, and a third mode of operation when the magnitude of current is greater than the second threshold wherein the semiconductor switch (18) is alternately pulsed conductive and non-conductive to limit the current through the load (14) to less than the second threshold, the control circuit (26) measures the pulses (74) to determine whether a parallel arc fault has occurred, when the measured pulses (74) are... ... when the magnitude of current is greater than the first threshold and less than a second threshold wherein the semiconductor switch (18) is rendered non-conductive after a predefined period of time, and a third mode of operation when the magnitude of current is greater than the second threshold wherein the semiconductor switch (18) is alternately pulsed conductive and non-conductive to limit the current through the load (14) to less than the second threshold, the control circuit (26) measures the pulses (74) to determine whether a parallel arc fault has occurred, when the measured pulses (74) are within a predetermined range a parallel arc fault is declared wherein the semiconductor switch (18) is rendered non-conductive.... ... when the magnitude of current is greater than the first threshold and less than a second threshold wherein the semiconductor switch (18) is rendered non-conductive after a predefined period of time, and a third mode of operation when the magnitude of current is greater than the second threshold wherein the semiconductor switch (18) is alternately pulsed conductive and non-conductive to limit

the current through the load (14) to less than the second threshold, the control circuit (26) measures the pulses (74) to determine whether a parallel arc fault

5/3,K/2 (Item 2 from file: 350) Links
Derwent WPIX

0010237223 & & *Drawing available*
WPI Acc no: 2000-548857/200050
Related WPI Acc No: 2000-506033; 2000-646885; 2000-647486; 2001-060711; 2001-070448; 2002-416386; 2005-381397
XRPX Acc No: N2000-406062
Asymmetric cryptographic processing system for providing security in digital communication network, has keys to respectively perform asymmetric and asymmetric cryptographic processing operations, at various rates
Patent Assignee: GEN INSTR CORP (GENN)
Inventor: ANDERSON S E; FELLOWS J A; MEDVINSKY A; MORONEY P; SPRUNK E J
Patent Family (6 patents, 86 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2000045546	A2	20000803	WO 2000US2170	A	20000128	200050	B
WO 2000045546	A1	20000803	WO 2000US2170	A	20000128	200050	B
AU 200033520	A	20000818	AU 200033520	A	20000128	200057	E
KR 2001108150	A	20011207	KR 2001709555	A	20010728	200236	E
EP 1236303	A1	20020904	EP 2000911658	A	20000128	200266	E
			WO 2000US2170	A	20000128		
US 20050027985	A1	20050203	US 1999128772	P	19990409	200511	E
			US 2000546900	A	20000410		
			US 2004893047	A	20040715		

Priority Applications (no., kind, date): US 1999117788 P 19990129; US 1999128772 P 19990409; US 2000546900 A 20000410; US 2004893047 A 20040715

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2000045546	A2	EN	21	3		
National Designated States,Original	AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW					
WO 2000045546	A1	EN	21	3		
National Designated States,Original	AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW					
AU 200033520	A	EN			Based on OPI patent	WO 2000045546
EP 1236303	A1	EN			PCT Application	WO 2000US2170
					Based on OPI patent	WO 2000045546
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
US 20050027985	A1	EN			Related to Provisional	US 1999128772
					Continuation of application	US 2000546900

Alerting Abstract ... ADVANTAGE - The approach of using keys of escalating levels of security to replace lower security keys is followed as many times as desired, to create a hierarchy of public key uses, with the result that the lower security operation is performed quickly, while the overall... Original Publication Data by AuthorityArgentinaPublication No. ...Original Abstracts:provide a high level of security while still allowing fast processing of encrypted information. The lower-security level includes keys which are small in length, which are changed relatively often, and which require less or fewer resources... ... a key pair at a higher security level (i.e, longer length keys) than the lower-security level keys is used to transfer the new lower-security public keys to devices using those keys. The higher-security... ... coding operations (120), (124).This approach of using keys of escalating levels of security to replace lower-security keys, where the higher-security keys require more resources, are more secure, and are... ... provide a high level of security while still allowing fast processing of encrypted information. The lower-security level includes keys which are small in length, which are changed relatively often, and which require less or fewer resources to implement their functions (130), (134). When it is required... ... a key pair at a higher security level (i.e, longer length keys) than the lower-security level keys is used to transfer the new lower-security public keys to devices using those keys. The higher-security keys can, in turn, be changed at a frequency lower than the lower-security keys. The higher-security keys require a higher level of resources

to perform their coding operations (120), (124).This approach of using keys of escalating ... provide a high level of security while still allowing fast processing of encrypted information. The lower-security level includes keys which are small in length, which are changed relatively often, and which require less or fewer resources to implement their functions (130), (134). When it is required to change key pairs of low security, a key pair at a higher security level (i.e, longer length keys) than the lower-security level keys is used to transfer the new lower-security public keys to devices using those keys. The higher-security keys can, in turn, be changed at a frequency lower than the lower-security keys. The higher-security keys require... ... higher level of resources to perform their coding operations (120), (124).This approach of using keys of escalating levels of security to replace lower-security keys, where the higher-security keys require more resources, are more secure, and are replaced less often than the lower-security keys, can be followed as many times as is desired to create a hierarchy of public key uses with th...

5/3,K/3 (Item 3 from file: 350) Links
Derwent WPIX

0009806595 & & *Drawing available*
WPI Acc no: 2000-096223/200008
XRPX Acc No: N2000-074294
Unauthorized access control system for CPU with privileged state firewall in computer system
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: ASLAM T; MOUGHANNI C; MOYER W C
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6003133	A	19991214	US 1997972069	A	19971117	200008	B

Priority Applications (no., kind, date): US 1997972069 A 19971117

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6003133	A	EN	8	5	

Original Publication Data by AuthorityArgentinaPublication No. ...Original Abstracts:different security policies can be set for different types of privilege level changes. In one embodiment, a default time-out value provides protection for multiple types of privilege level changes. ...Claims:characterized as operating in a first mode and a second mode which is at a lower privilege level than said first mode;when in said first mode said central processing unit allows access to a protected system...

5/3,K/4 (Item 4 from file: 350) Links
Derwent WPIX

0008488284 & & *Drawing available*
WPI Acc no: 1998-017871/199802
XRPX Acc No: N1998-013674
Hand-held and hand-operated instrument - has keyboard with keys for different food exchange, 1st display for nutritional quantities, 2nd keyboard for entering user's weight and 2nd display for recommended daily caloric intake for losing set amount of weight per week
Patent Assignee: GUMP C (GUMP-I)
Inventor: GUMP C
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5691927	A	19971125	US 1994296759	A	19940826	199802	B

Priority Applications (no., kind, date): US 1994296759 A 19940826

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5691927	A	EN	18	6	

Original Publication Data by AuthorityArgentinaPublication No. ...Claims:said nutritional quantities is the approximate cumulative caloric level accumulated since a given starting time; second keyboard means, said second keyboard means comprising a plurality of keys; second calculating means, said second calculating means having means for rendering numerical manipulations in response...

5/3,K/5 (Item 5 from file: 350) Links
Derwent WPIX

0007215012 & & *Drawing available*
WPI Acc no: 1995-262599/199534
XRPX Acc No: N1995-201834; N1995-247307
Data processor for signal represented by symbols for transmission - converts each source of data bits into

symbols in different signal constellation, one of which has intersymbol separation different from that of another constellation
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: CHUNG H; CHUNG H Y; SORBARA M
Patent Family (6 patents, 6 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
TW 249873	A	19950621	TW 1994104875	A	19940528	199534	B
EP 674413	A2	19950927	EP 1995301753	A	19950316	199543	ETAB
JP 7273812	A	19951020	JP 199560283	A	19950320	199551	E
EP 674413	A3	19970507	EP 1995301753	A	19950316	199731	E
US 5901135	A	19990504	US 1994215562	A	19940321	199925	E
			US 1995547584	A	19951024		
			US 1997808703	A	19970228		
KR 338911	B	20021114	KR 19955827	A	19950320	200330	E

Priority Applications (no., kind, date): US 1994215562 A 19940321; US 1995547584 A 19951024; US 1997808703 A 19970228

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
TW 249873	A	ZH	5	7		
EP 674413	A2	EN	9	7		
Regional Designated States,Original	DE FR GB					
JP 7273812	A	JA	7			
EP 674413	A3	EN				
US 5901135	A	EN			Continuation of application	US 1994215562
					Continuation of application	US 1995547584
KR 338911	B	KO			Previously issued patent	KR 95035168

Original Publication Data by AuthorityArgentinaPublication No. ...Claims:a first desired level of error protection for the data bits from the first source, b) a second desired level of error protection for data bits from the second source, c) a first time delay no greater than a first amount of time for the data bits... ... amount of time and the first desired level of error protection is equal to the second desired level of error protection; andmeans for time-division-multiplexing the symbols of said data signal.

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